



SFF SDR development platforms FAQ 1.0

This document presents the most frequently asked questions about the SFF SDR development platforms.

SFF SDR development platforms

What is the overall power consumption of the SFF SDR development platforms?

- The overall power consumption of the SFF SDR Development Platform running the supplied FRS example is approximately 20 W.
- The overall power consumption of the SFF SDR Evaluation Module running the supplied DSP/FPGA loopback example is approximately 6 W.

What is the power consumption of individual modules of the SFF SDR development platforms?

- Digital Processing Module: approximately 6 W (running a DSP/FPGA loopback)
- Data Conversion Module: approximately 14 W (at maximum sampling rates and gains)
- RF Module: approximately 4 W

Digital Processing Module

What are the possible transfer rates between the DSP and the FPGA?

Although preliminary, the following results were obtained in burst mode (*i.e.* when transferring one frame between the DSP and the FPGA).

- FPGA to DSP (referred to as VPFE): 150 MBps (16 bits, 75 MHz).
- DSP to FPGA (referred to as VPBE): 75 MBps (16 bits, 37.5 MHz).

Note

Sustained transfer rates will become available at a later date.

What is the maximum transferable frame size through the VPSS?

The maximum frame size is 512 samples of 32 bits each, or 1024 samples of 16 bits each.

Is it possible to stream data through Ethernet or USB?

Streaming data through Ethernet and USB is not supported at present.

Note

Specifications regarding these types of streaming will become available at a later date.

What processors may developers target with the model-based design flow (MBDK)?

The DSP side of the DM6446 and the Virtex-4 SX35 FPGA of the Digital Processing Module can be targeted.

What processors may developers target with the language-based design flow (BSDK)?

The ARM side of the DM6446 (some conditions apply; see the next question for details), the DSP side of the DM6446, and the Virtex-4 SX35 FPGA of the Digital Processing Module can be targeted.

Is it possible to target the ARM to perform user-defined processing?

Because the ARM runs the INTEGRITY real-time operating system (RTOS) and that all the drivers on the ARM are designed for INTEGRITY, targeting the ARM is only possible through the language-based design flow and the MULTI integrated development environment (IDE). In other words, the ARM cannot be targeted through the model-based design flow. The following is a brief description of the components running on the INTEGRITY RTOS.

- Ethernet management
- Central communications engine (CCE)
- ARM/MSP430 communications (manages power monitoring)
- File system management
- Startup sequence and initialization

The following I/O are controlled by the DSP:

- Audio codec
- DSP/FPGA communications (VPSS)
- RF Module configuration and control
- Data Conversion Module configuration and control

Are the SFF SDR development platforms offered with different FPGA?

Lyrtech does not offer FPGA models other than the Virtex-4 SX35 in the case of single-unit orders. In the case of bulk orders, however, Lyrtech can accommodate. Contact Lyrtech for details.

What are the depths of the FIFO on each side of the FPGA?

The FIFO connecting the ADC and DAC to the FPGA have a 16-sample depth for retiming purposes. The FIFO connecting the DSP to the FPGA have a depth of 1024 samples. The FIFO all have a width of 32 bits.

What components and interfaces of the SFF SDR development platforms may be controlled?

The following list of components and interfaces can be controlled through the DSP with both design flows:

- Audio codec
- LED
- Push buttons
- DIP switches
- DSP-FPGA data bus
- DSP-FPGA registers
- Power monitoring
- Data Conversion Module (sampling frequencies, TX and RX programmable amplifiers, on and off, clock source, interpolation factor)
- RF Module (TX and RX local oscillator frequency, on and off, onboard and external clock sources, IF bandwidth, oscillator lock status)

Is the MULTI IDE from Green Hills Software essential to developing applications on the SFF SDR development platforms?

The MULTI integrated development environment and tools suite from Green Hills Software can be used to target the ARM portion of the DM6446 running the INTEGRITY RTOS and to target the DSP portion of the DM6446. Although it may be necessary to deploy an SCA waveform for the SFF SCA Development Platform, it is not necessary to the SFF SDR Evaluation Module or the SFF SDR Development Platform.

How is it possible to interface expansion boards to the Digital Processing Module?

Lyrtech does not offer optional expansion boards at this time. However, in the near future, it will be possible to connect third-party modules to the SFF SDR development platforms through their GPIO, RS232, Hi-speed USB, and Ethernet ports.

Can the SDRAM be upgraded beyond 128 MB?

The DDR2 SDRAM cannot be upgraded beyond 128 MB.

Can the SD memory card be used for data recording purposes?

Although it is not supported at present, in the near future, the SD memory card will be used to record and play back data in both design flows.

How much processing power does the Digital Processing Module deliver?

The ARM926 core is clocked at 296 MHz. It can process multiply-accumulate operations in single-cycle instructions. The C64+ DSP core can process 4752, 8-bit MMAC or 2376, 16-bit MMAC at

594 MHz. The Virtex-4 SX35 FPGA has 15,360 CLB slices, 192 18-kilobit blocks of RAM, and 192 XtremeDSP slices.

What is the capacity of the FPGA before waveform functions are added?

At this time, 85% of the Virtex-4 SX35 FPGA resources are available.

Data Conversion Module

How do I know if the signal I am trying to acquire is out of range?

A red LED at the front of the Data Conversion Module (on the same side as the connectors) indicates whether the ADC is saturated.

Is the Data Conversion Module sold separately as a stand-alone product?

The Data Conversion Module is only offered as part of the SFF SDR Development Platform.

If I acquire the SFF SDR Evaluation Module, is it possible to upgrade it to an SFF SDR Development Platform?

Yes. An upgrade option appears on version 1.1 of the Lyrtech price list.

Is it possible to control the amplitude of the analog signal before analog-to-digital conversion?

A programmable gain amplifier and a programmable attenuator (located before the ADC) can be controlled from the DSP. The programmable gain amplifier has a 20-dB range (between 10 dB and 30 dB) and it can be tuned in by increments of 1.5 dB. The programmable attenuator has a 15.5-dB range (between -15.5 dB and 0 dB) and it can be tuned by increments of 0.5 dB. This combination provides an overall range of 35.5 dB. The components are controlled through the DSP API of the supplied board software development kit (BSDK) or the DSP blockset of the model-based design kit (MBDK).

Is it possible to control the amplitude of the analog signal after analog-to-digital conversion?

A programmable gain amplifier is integrated to the DAC. It has an approximate range of 25 dB. The component is controlled through the DSP API of the supplied BSDK or DSP blockset of the MBDK.

What are the signal-to-noise ratio and spurious-free dynamic range of the analog-to-digital converters?

The complete characterization of the components has not yet been completed. The following are preliminary measurements with a 70-MHz tone at 125 MSPS:

- SNR: 57 dB
- SFDR: 73 dB

What are the nominal levels of the ADC and DAC?

- ADC: -7 dBm input with a minimum gain and no attenuation
- DAC: 0 dBm

How is the Data Conversion Module controlled?

The Data Conversion Module can be controlled with the functions of the supplied API or the Simulink blocks associated to the module.

Is it possible to implement signal processing in the FPGA of the Data Conversion Module?

No. It is not possible to do so at this time.

Is it possible to stack several Data Conversion Modules?

As there is only one Data Conversion Module expansion port on the Digital Processing Module and the Data Conversion Module, the Digital Processing Module only supports one Data Conversion Module.

Is there useable RAM on the Data Conversion Module?

No, there is not.

Is there analog automatic gain control before the analog-to-digital converters?

There is no analog automatic gain control before the ADC because such control is waveform-dependant, making it preferable to implement it in software and have it control the programmable gains located immediately before the ADC.

What are the power requirements of the Data Conversion Module?

The Data Conversion Module requires 3-V, 5-V, and 12-V supplies.

Are the ADC and DAC clocks independent?

When using the product in external clock mode, ADC and DAC clocks may have independent sources. When using the product in onboard clock mode, the ADC and DAC clocks may have different frequencies, but there must be an integer ratio between them because they have the same source.

What amplifier is used for the programmable reception gain?

You can tune the signal level through the PE4305 programmable attenuator and the LT5514 programmable gain amplifier.

Is there a synchronization input on the Data Conversion Module?

When using the product in onboard clock mode, a *sync* signal may be input through one of the module's SMA connectors.

RF Module

How is the RF Module controlled?

The RF Module can be controlled with the functions of the supplied API or the Simulink blocks associated to the module.

Are there probing points on the RF Module?

No. There are not. The signals can, however, be probed between the RF Module and the Data Conversion Module.

How many RF modules can be simultaneously interfaced to the SFF SDR Development Platform?

The Data Conversion Module of the SFF SDR Development Platform has two RX channels and two TX channels. The default RF Module uses one ADC channel and two DAC channels (because TX requires quadrature). Logically, a second RF Module could be used simultaneously, but only its RX path would be usable. Using single-ended interface third-party RF modules with the Data Conversion Module could allow two RF modules to be used simultaneously.

How many channels equip the RF Module?

The RF Module is equipped with one transmission channel and one reception channel.

Is it possible to transmit and receive simultaneously?

The SFF SDR Development Platform can transmit and receive simultaneously because it is full-duplex. TX and RX frequencies are also independent.

What is the frequency range of the supplied antennas?

The antennas supplied with the SFF SDR Development Platform are tuned to operate between 450 MHz and 490 MHz, covering the FRS and GMRS bands.

Is it possible to use other antennas than the ones supplied?

You can connect any other antenna to the SFF SDR Development Platform. The RF Module is equipped with standard female SMA connectors. Two standard male-to-male SMA 90° elbows are also supplied with the platforms.

What is the maximum input power that the RX path can sustain?

The maximum power level before compression is -10 dBm. The nominal power level at the RX antenna is -25 dBm.

The RF Module shows a 12-V power input. What is the required current?

The RF Module draws approximately 330 mA.

What is the shape factor of the 5-MHz and 20-MHz filters?

Specification	BPF1	BPF2
Center frequency	300 MHz	300 MHz
Bandwidth	5 MHz	20 MHz
Insertion loss	Maximum of 10 dB	Maximum of 10 dB
Pass band	Less than 3 dB (297.5 MHz and 302.5 MHz)	Less than 3 dB (290 MHz and 310 MHz)
Ripple	Maximum of ± 0.5 dB	Maximum of ± 0.5 dB
Stop band	More than 35 dB (290 MHz and 310 MHz) More than 50 dB (270 MHz and 330 MHz)	More than 20 dB (280 MHz and 320 MHz) More than 50 dB (270 MHz and 330 MHz)
Input/output impedance	50 Ω	50 Ω

What are the reception noise figure and transmission signal-to-noise ratio?

Figures to come at a later date.

What are the transmission and reception gains of the RF Module?

- Transmission gain: 0 dB
- Reception gain: 25 dB

What is the phase noise of the RF Module?

Figures to come at a later date.

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